We claim:

1. **A process** for the firm connection of processed semiconductor wafers, preferably for connecting system wafers (1) supporting microelectromechanical or electronic structures with cover wafers (2), which, preferably also support electronic structures, wherein, in the case of more than two wafers, the wafers located in a central area of the stack are in particular simultaneously both system wafer and cover wafer, wherein in an operation of a mechanically firm connecting both electrically insulating connections (6, 6a, 6b) and electrically conductive connections (5) are produced between the semiconductor wafers, said process comprising at least the following specific main operations

   - applying structured layers of electrically non-conducting and electrically conducting glass paste on respectively one of the two wafer sides to be connected with each other;
   - conditioning and premelting of the glasses or glass pastes (5, 6);
   - geometrical alignment of the wafers to be connected;
   - joining, in particular bonding, of the wafers at a processing temperature of the glasses or glass pastes using mechanical pressure.

2. The process according to claim 1, characterized in that the glass pastes, in particular glass solders are applied with a screen printing process.

3. The process according to claim 1, characterized in that the non-conducting, low-melting glass paste and the electrically conducting glass paste have different conditioning and premelting conditions and that, consequently, the conditioning and premelting are implemented successively in a respectively separate process.

4. The process according to claim 1, characterized in that the non-conducting, low-melting glass paste and the electrically conducting glass paste have substantially the same processing temperature.

5. The process according to claim 1, characterized in that the non-conducting, low-melting glass paste and the electrically conducting glass paste have different processing temperatures and these are successively passed in a process.

6. The process according to claim 1 and any of claims 2 to 5, characterized in that at least one of the wafers is electrically connected in an area that is not structured electronically (area of the starting material).

7. The process according to claim 1 and any of claims 2 to 6, characterized in that the wafers are electrically connected at specific switching points in their electronically structured areas (3).

8. The process according to claim 1 and any of the subsequent claims, characterized in that the formation of the connections of the glass pastes takes place at a temperature of less than 450°C.

9. The process according to claim 1 and any of the subsequent claims, characterized in that the electric connection of the substrate for SOI wafers is implemented through previously produced openings in a buried oxide layer and in an active silicon layer, in particular the wall areas of the opening in the active silicon layer being provided with an insulating layer (7a) prior to the electric connection.

10. **Wafer arrangement** which was produced or can be produced according to the process according to claim 1 or a process of the subsequent claims.

11. **A process** for the firm connection of processed semiconductor wafers, preferably for connecting a system wafer (1) supporting microelectromechanical or electronic structures with a cover wafer (2) which, in particular also supports electronic structures, wherein in an operation of a mechanically firm connecting both electrically insulating connections and electrically conductive connections are produced between the semiconductor wafers, said process comprising at least the following specific main operations

    - applying a first electrically non-conducting, structured layer and a second electrically conducting layer of respectively one glass paste (5, 6) on at least one of the two wafer (1, 2) to be connected with each other;
    - conditioning of the glass pastes (5, 6);
    - premelting of the conditioned glass pastes (5, 6);
    - geometrical alignment of the wafers (1, 2) to be connected;
    - joining, in particular bonding, of the wafers (1, 2) at a processing temperature of the glass pastes using mechanical pressure.

12. The process according to claim 11, wherein the glass pastes (5, 6), in particular glass solders, are applied with a screen printing process.

13. The process according to claim 11, wherein the non-conducting, low-melting glass paste (6, 6a) and the electrically conducting glass paste (5) have different conditioning and/or premelting conditions and that, consequently, the conditioning and premelting of each of the pastes are implemented successively in a respectively separate process.

14. The process according to claim 11, wherein the non-conducting, low-melting glass paste (5) and the electrically conducting glass paste (6) have substantially the same processing temperature.

15. The process according to claim 11, wherein the non-conducting, low-melting glass paste (5) and the electrically conducting glass paste (6) have different processing temperatures and these are successively passed in a process.

16. The process according to claim 11, wherein at least one of the wafers is electrically connected in an area not structured electronically (area of the starting material).

17. The process according to claim 11, wherein at least one of the wafers is electrically connected at specific switching points in their electronically structured area(s) (3).

18. The process according to claim 11 and any of the subsequent claims, wherein the formation of the connections of the glass pastes takes place at a temperature of less than 450°C.

19. The process according to claim 11 and any of the subsequent claims, wherein the electric connection of a substrate (11) of an SOI wafer (8) is implemented through at least one previously produced opening in a buried oxide layer (10) and in an active silicon layer (9), in particular the wall areas of the opening in the active silicon layer being provided with an insulating layer (7a) prior to the electric connection (5) with the conducting glass solder.

20. **A process** for the firm connection of processed semiconductor wafers, preferably for connecting system wafers (1) supporting microelectromechanical or electronic structures (3) with cover wafers (2) which may also support electronic structures, wherein in the case of more than two wafers the wafers located in a central area of the stack are simultaneously both system wafer and cover wafer, wherein in an operation of a mechanically firm connecting both electrically insulating connections and electrically conducting connections are produced between the semiconductor wafers, characterized by the following specific main operations

- applying structured layers of electrically non-conducting and electrically conducting glass pastes on respectively one of the two wafer sides to be connected with each other;
- conditioning and premelting of the glasses (5, 6);
- geometrical alignment of the wafers to be connected;
- joining (bonding) of the wafers at the processing temperature of the glasses using mechanical pressure.

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